Imbedded Component / Die Technology: An Innovative Packaging Solution for High Reliability

Casey Hatcher
Soldering Technology International, Inc.
Madison, AL USA
chatcher@solderingtech.com

Originally published in the Proceedings of the Pan Pacific Microelectronics Symposium, Oahu, Hawaii, February 10-12, 2004.

ABSTRACT

The need for increased reliability coupled with reduced size and weight has demanded the evolution of technology for assembling printed circuit boards. Imbedded Component / Die Technology (IC/DT)™ will advance electronics packaging to the next level in the 21st century by transforming 2-Dimensional(2D) component assembly and placement into 3-Dimensions (3D). Imbedded Component / Die Technology substitutes placement of components on the surface of an organic substrate onto or near a rigid, thermally conductive core utilizing multi-level cavities. The elimination of all external component level packaging further increases reliability by reducing the number of opportunities for electrical and mechanical failure. The use of bare die and thin/thick film components reduces both overall mass/weight and circuit card assembly (CCA) size. Imbedded Component / Die Technology improves form factor with increased component-to-substrate ratio allowing for smaller CCA's or for the addition of redundant systems to increase reliability for high reliability (Hi-Rel) applications. Flexible interconnects from component-to-component or component-to-substrate, coupled with a vibration-dampening encapsulant, allow for reliable use in high mechanical shock and vibration environments. Replacing solder as the mechanical and electrical attachment material, conductive adhesives and wire bonds allow for lower overall processing temperatures. The use of Imbedded Component / Die Technology when assembling CCA's can dramatically improve reliability and also improve form factor.

KEYWORDS: Wire Bonds, Conductive Adhesives, Organic Substrate, Reliability, Hi-Rel, 3-Dimensional, Cavities, Thermal Core, Imbedded Components, Bare Die

INTRODUCTION

Board assembly has evolved from the first electronics packaging technology, single-sided through-hole mount assembly (THMA), in the 1940's to the current packaging technology using surface mount (SMT) beginning in the 1970's [1]. Research is continually conducted in order to reduce circuit card assembly (CCA) weight and size while increasing functionality. New technologies are required to achieve these goals as CCA's have reached maximum density utilizing double-sided SMT. High Reliability (Hi-Rel) requirements for assemblies demand that CCAs survive harsher environments for longer working lives. The need to reduce form and fit factor while increasing the number of thermal shock, mechanical shock, and vibration cycles has demanded the development of a revolutionary method of packaging electronics.

The concept of imbedding components in laminate for increased reliability in addition to reducing CCA size and weight has been tried and tested unsuccessfully for many years by large integrated circuit (IC) companies. However, recent developments at Soldering Technology International have led to the successful assembly and testing of a laminate CCA with imbedded components. Imbedded Component / Die Technology (IC/DT™) allows for the highest component-to-substrate ratio by using a 3-Dimensional (3D) approach to assembling CCAs. Like THMA and SMT, components are populated on an organic laminate substrate. Unlike these two aging technologies, active and passive devices may be placed on multiple layers within the laminate printed circuit board (PCB) using IC/DT™. With the development of any new packaging technology, new or conforming components are synonymous with the technology. Just as radial leaded and dual in-line packages (DIP's) have evolved into surface mount devices (SMD), IC/DT™ utilizes components with all external packaging removed (i.e. bare die and thick/thin film components). Unlike THMA and SMT, IC/DT™ utilizes thermally conductive adhesives and wire bonds as the mechanical and electrical connections. IC/DT™ addresses thermal management by placing high power dissipative devices on an underlying cooling core. This core also provides a rigid platform for allowing components to withstand high-G and vibration environments. All of the above features coupled together make for the smallest form/fit factor, Hi-Rel CCA.

FEATURES AND ADVANTAGES

Imbedded Component / Die Technology improves long-term reliability by eliminating unnecessary failure opportunities and utilizing reliable electrical interconnects. All external component packaging, as well as solder joints, are eliminated. Bare die are utilized and imbedded into an organic, laminate substrate and attached to a rigid cooling core. The core adds mechanical stability while eliminating the need for additional thermal management materials such as heat sinks and fans. Flexible electrical interconnects provide a reliable means of connecting input/output (I/O). Substrate area previously occupied by external packaging, bulky solder joints, and/or thermal management materials

can now be eliminated or repopulated with the addition of supplementary features or redundant systems. Additional environmental protectants are used to protect the internal components from the environment creating a reliable, robust package.

Mechanical Characteristics

Mass savings using Imbedded Component / Die Technology are to a large extent attributable to the elimination of secondary packaging material. IC/DT™ utilizes bare die and hybrid passive components that are wire bondable. Since the IC/DT™ design creates a protected environment in which to use components in bare die form, the external packaging of the component is no longer required. Overmold material and interconnect materials that typically connect the output of the bare die IC to the external system on the PCB are eliminated. Interconnect materials, dependant upon the component package, include lead frame, pins, interposers, additional wire bonds, and/or solder spheres.

In addition to the reduction in component packaging mass, there is also a reduction in the mass related to the attachment material. Conventionally, solder serves as the attachment material between a component lead frame and the corresponding substrate pad or plated-through-hole (PTH). A significant mass savings is achieved by using wire bonds rather than solder because of the decreased volume of material per connection, as well as the lower density of typical wire bond materials compared to eutectic (Sn63/Pb37) solder. Analytical modeling of a 325 I/O device in a conventional package configuration such as quad flatpacks (QFP) and ball grid arrays (BGA) predicts an attachment material volume 142 times that required for the wire bonded IC/DT™ equivalent component in die form. This coupled with a 72% reduction in the density of the attachment material translates into a 99% reduction in attachment material mass as shown in Table 1.

Table 1. Mass savings per electrical connect method.

Type of Interconnect	QFP	BGA	Thermosonic Ball	Ultrasonic Wedge
Interconnect Material	Solder Paste (0.03" x 0.1" x 0.006")	Solder Balls (0.03" Diameter)	Gold Wire Bond (0.00125" Diameter)	Aluminum Wire Bond (0.0012" Diameter)
Volume per Connection (cm^3)	0.09586	0.07529	0.00065	0.00060
Density (g/cm^3)	9.630	9.630	19.300	2.696
Total Mass (g)	0.9232	0.7251	0.0126	0.0016

Not only has analytical modeling illustrated the reduction in attachment material mass, but also the increased flexibility of the electrical attachment further improves the reliability of the end product. By using wire bonding technology as the electrical attachment process, very flexible interconnects are created. This flexibility is exploited during operation in demanding mechanical environments such as vibration or mechanical shock. In contrast to a soldered connection, which localizes the applied stress, the IC/DT™ concept distributes the applied stress producing a more robust and rugged electrical product. Coupled with the vibration-dampening matrix of encapsulation material to reduce the effects of wire bond resonance, the long-term reliability of a CCA is greatly increased.

In addition to the stress relieving characteristics of the flexible connections, the cooling core serves a dual role by providing mechanical rigidity to reduce the overall board deflection during external loading. This reduction in board deflection greatly enhances the robustness of the end product by reinforcing the CCA assembly for mechanical shock and vibration in its most susceptible axis.

Lowering the z-axis component height is paramount in importance of IC/DT™ to increasing the reliability of the end product. Reduced component heights, along with the lower component mass concentrations, decrease the mechanical stress/strain on the attachment interfaces during mechanical shock and vibration. As Figure 2 illustrates, the large z-axis height of populated packages including multi-chip modules (MCM's) increases the susceptibility of the mechanical/electrical interconnect to fracturing and subsequent failure due to the leveraging of forces associated with the high center of gravity of the assembly. By lowering the center of gravity to a rigid core and by distributing the applied stress along the flexible electrical attachments, the overall assembly reliability is greatly increased.

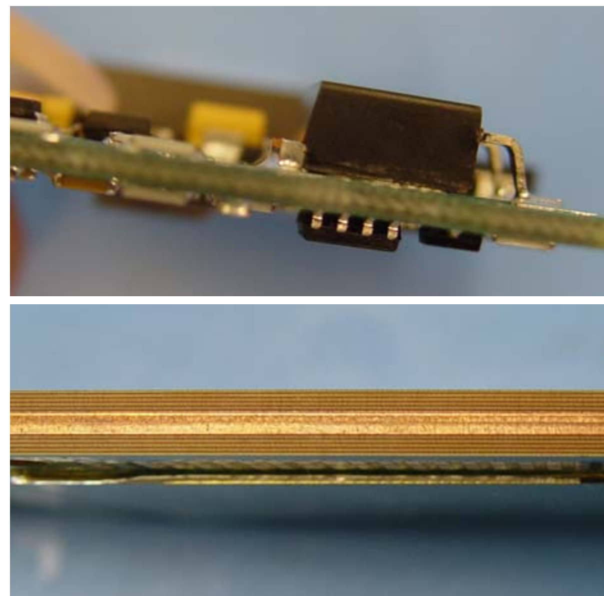

Figure 2. (a) High profile components assembled on typical THM or SMT board. (b) Significant height reduction, dual substrate assembly using IC/DT™ (Source: STI).

Thermal Characteristics

Fundamentally, the Imbedded Component / Die Technology design concept produces challenges with thermal management on high power dissipating devices. Conventionally, a heat generating CCA would dissipate heat through convection or radiation from the component

surfaces, often including a package level heat sink. IC/DT™ inhibits those modes of heat transfer by isolating the heat dissipating components from the environment with encapsulation. Therefore, IC/DT™ relies on conduction to a single, central cooling core to remove heat from high power devices and distributes the heat evenly along the interface. Conversely, this central core may also be used as an internal PCB heater for space applications to maintain functional operating temperatures. Heat generating devices may strategically be placed on the core to dissipate power/heat for stabilizing the overall substrate temperature.

Thermal imaging of design modules has illustrated the dramatic reduction in "hot spot" temperature when comparing power-dissipating transistors. Testing of a conventional through-hole transistor component, Figure 3, compared to the same bare die transistor mounted to the

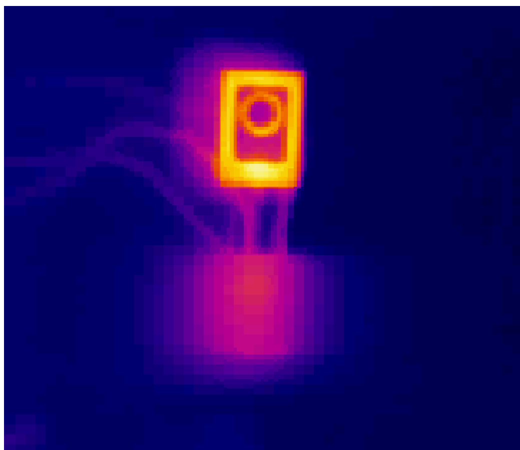

Figure 3. Through-hole transistor in TO-32 case with local temperatures of 163ºC (Source: STI).

IC/DT™ cooling core, Figure 4, yielded an 80% reduction in localized hot spot temperature when mounted to the IC/DT™ cooling core. This elimination of the localized heat directly reduces the potential for thermal related component failures, and subsequently increases the reliability of the overall CCA.

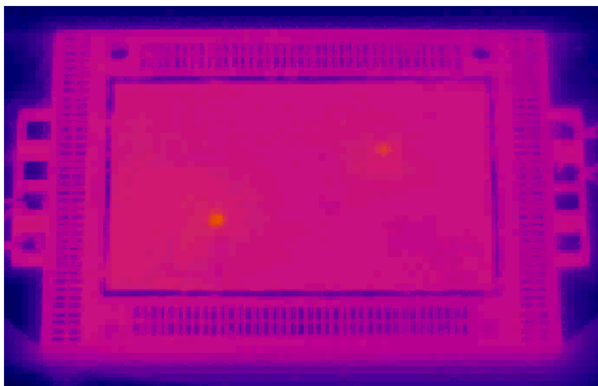

Figure 4. Imbedded transistors in IC/DT™ design module with maximum local temperatures of 32ºC (Source: STI).

Materials Characteristics

Imbedded Component / Die Technology requires a unique set of materials to successfully imbed components into an organic substrate. For Hi-Rel applications, a high-performance, tetrafunctional FR-4 epoxy laminate and prepreg system is selected. This laminate has a low dissipation factor and dielectric constant for improved signal propagation. Additionally, the high-performance FR-4 has a high glass transition temperature (Tg) for maintaining a stable, low coefficient of thermal expansion (CTE). The x/y-axis CTE of this material is minimized for reducing CTE mismatch between the silicon die coupled to the substrate for extended reliability.

Adhesive die attach material is used for mechanically coupling the components to the organic substrate. Thermally conductive adhesives provide a good alternative to solder due to a reduction in density/mass and lower processing temperatures. This low modulus adhesive compensates for the mismatch in CTE between the substrate and components. An electronic grade polymer is used to prevent introduction of ionic contaminants in the assembly which aid in the corrosion of interconnects and components. Adequate volume of the material is dispensed so that a fillet forms around the perimeter of the component for optimal adhesion strength. Dispense parameters are optimized to insure excess epoxy does not bleed-out and wick two adjacent components together or obstruct bond pads.

Conductive adhesives serve as mechanical and electrical connections with the addition of a filler material such as silver. The silver filler particles also enhance the thermal conductivity of the die attach material. By eliminating solder as the electrical interconnect, the cleaning process step is eliminated since there is no remaining flux residue. An isotropic, conductive adhesive with a volume resistivity comparable to solder is selected. This silver-filled adhesive is highly thermally conductive for attaching components with elevated power dissipation levels. Low levels of ionic contaminants in the material reduce corrosion opportunities. Both electrically conductive and non-electrically conductive adhesives are cured quickly at low temperatures. The die attach cure temperature is the thermal ceiling of the overall assembly process reducing the potential for latent thermal related failures.

Imbedded components synonymous with IC/DT™ include bare die and thick/thin film components. Bare die are thin film IC's fabricated today on a wide variety of substrate material. The most prevalent material still remains Silicon (Si) as it is plentiful and inexpensive. All die are available with wire bondable surfaces, typically Copper (Cu) doped Aluminum (Al) for either component level assembly or substrate level assembly. Passive devices are available in a wide range of substrate materials and metallization schemes for various attachment methods. Advances in technology have enabled the dramatic reduction in the size of passives by fabrication on Si substrates using thin film deposition. Thick and thin film end-termination passive devices on

various ceramic substrates are also widely available. A vast array of metallization schemes can be deposited dependant upon the electrical and/or mechanical attachment method.

Flexible interconnects such as wire bonds provide reliable electrical pathways from a component/die to either another component/die or to the PCB. Wire bonding is a proven reliable method for connecting component I/O. A plasma clean prior to bonding ensures that all surfaces are contaminant and oxide free. This increases bondability and long-term reliability of the wire bond. The wedge bonding technique is recommended using an alloy of Al wire. Ultrasonic energy and mechanical force form the first and second bond, also known as the stitch, at room temperature. Substrate bond pads/traces composed of Cu/Ni/Au are typically used with Al alloy wire [2]. The Al bonds through the Au to the nickel (Ni) for a reliable bond, while the Au protects the bond pad from oxidation. Small diameter wire, 1.2 mil, is used for low current applications, while large diameter wire, 5 mil, is used for high current. Kirkendall voiding and corrosion is minimized by maintaining low processing temperatures, low levels of ionic contaminants, and a near hermetic environment within the substrate.

Two additional materials are used during the IC/DT™ assembly process to provide environmental protection as well as maintain electrical integrity. A conformal coating such as Parylene is applied to render all surfaces electrically insulating and protect against moisture and contaminates. Parylene is vapor deposited at room temperature onto the substrate additively over time. Due to the method of application, Parylene offers complete and uniform coverage including edges and sharp corners without bridging between adjacent surfaces. Parylene improves die shear strength and wire bond pull strength up to 900%. Unlike other polymeric materials, Parylene forms a near hermetic seal with extremely low moisture absorption and moisture vapor transmission. Parylene is resistant to chemical attack or breakdown up to 150°C.

Another environmental barrier applied after Parylene deposition is an encapsulant to provide additional protection from the PCB's external environment. A silicone gel encapsulant is dispensed into each cavity. This two-part gel provides vibration dampening for the wire bonds due to its low modulus. The encapsulant is readily used in bare die applications and contains low levels of ionic contaminates. The gel retains its low modulus over a wide temperature range due to an extremely low Tg. The encapsulant bonds well to all surfaces and also provides an alternate method of thermal dissipation.

Once the encapsulation is applied, a Cu shield is then used as a final means of environmental protection to seal the cavities from the external environment. The Cu lid provides electromagnetic interference (EMI) shielding as well as physical protection from foreign objects. This material matrix is designed to enhance the overall robustness of the CCA by imbedding the electronics in a protected encasement.

Electrical Characteristics

Imbedded Component / Die Technology improves long-term signal reliability by eliminating unnecessary failure opportunities and utilizing reliable electrical interconnects. High density interconnects for complex circuits are realized using IC/DT™. All external component packaging, as well as solder joints, are replaced with a more reliable electrical interconnect. Unnecessary interconnections can further be reduced by bonding from component to component. Signal integrity is maintained with the use of large ground and power planes.

Similar to chip-on-board (COB), IC/DT™ utilizes chip and wire technology for integrating IC's into a CCA. Wire bonding is a mature and robust technology that has been around since the 1960s. Much research has been conducted for determining reliability of wire bonds and understanding their electrical characteristics. Only one electrical interconnect method has less electrical parasitics than wire bonds – flip chip [2]. However, small-diameter solder spheres lack the mechanical/electrical reliability in Hi-Rel applications that wire bonds can offer.

For increased signal reliability, all first level component packaging is eliminated. This reduces two to four possible modes of electrical failure associated with component level packaging. A QFP is shown in Figure 5 with three additional conductors that could result in points of failure. Additional traces on the interposer, wire bonds from the interposer to a lead frame, and the solder connection

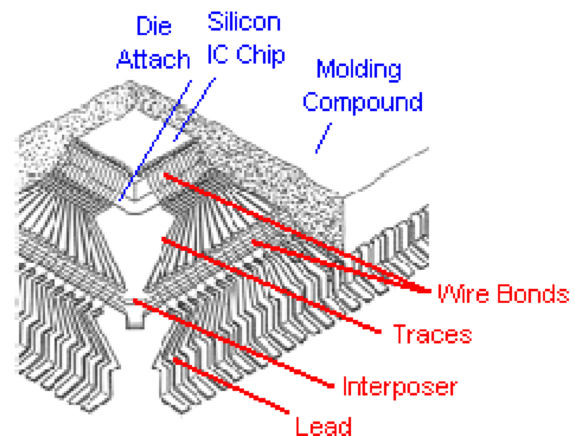

Figure 5. Component-level packaging of a QFP (Source: STI).

between the lead frame and substrate are all possible points for an electrical defect. Another typical component package, the BGA, is also shown in Figure 6 with three additional conductors or failure opportunities. These conductors include wire bonds from the IC die to an interposer, traces on the interposer to solder spheres underneath the interposer, and the solder interconnect

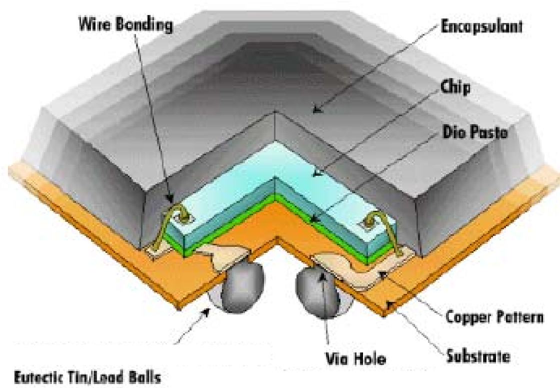

Figure 6. Component-level packaging of BGA (Source: Terman [3]).

between the spheres to the substrate bond pad. Reducing the number of interconnects from an IC's output to the circuit on the substrate eliminates failure opportunities.

Eliminating external packaging also reduces parasitic transmission line parameters from the component to the substrate. Parasitic resistance, inductance, and capacitance are added with each conductor used to interconnect the IC's output signal to the PCB. Increased parasitics results in attenuation of signals and crosstalk. The pin grid array (PGA) shown in Figure 7 contributes parasitics due to traces on an interposer as well as pins connecting the interposer to the substrate. These conductor's parasitics, determined by material used and conductor geometry, can add 3x to 14x additional inductance and capacitance to the circuit over a single wire bond interconnect. The BGA previously shown contributes parasitics due to traces on an interposer as well as large solder spheres connecting the interposer to the substrate. These parasitics can add 2x to 8x additional inductance and capacitance to the signal path. A DIP contributes parasitics due to a lead frame as well as pins connecting the lead frame to the substrate. These parasitics can add 4x to 30x additional inductance and capacitance to the signal path [3]. Not only are failure opportunities eliminated using IC/DT™, but electrical parasitics are minimized as well.

The IC/DT™ substrate and cavity design promotes optimum electrical performance. Placement of components in cavities allows wiring of high-density components by providing multiple tiers for bonding signal and power/ground connections. Staggered bond pads on the substrate maintain bond wire pitch between the die and substrate, reducing fan-out. Cavity dimensions are kept to a minimum for reducing distances between die bond pads and substrate tier bond pads maintaining short wire bond lengths. Wire bond parameters such as resistance, inductance (both mutual and self), and capacitance (both mutual and self) are minimized by reducing conductor length. Multiple components, both die and thick film end-termination components, imbedded in the same cavity allow for close physical placement. Component-to-component bonding is made possible therefore reducing signal path

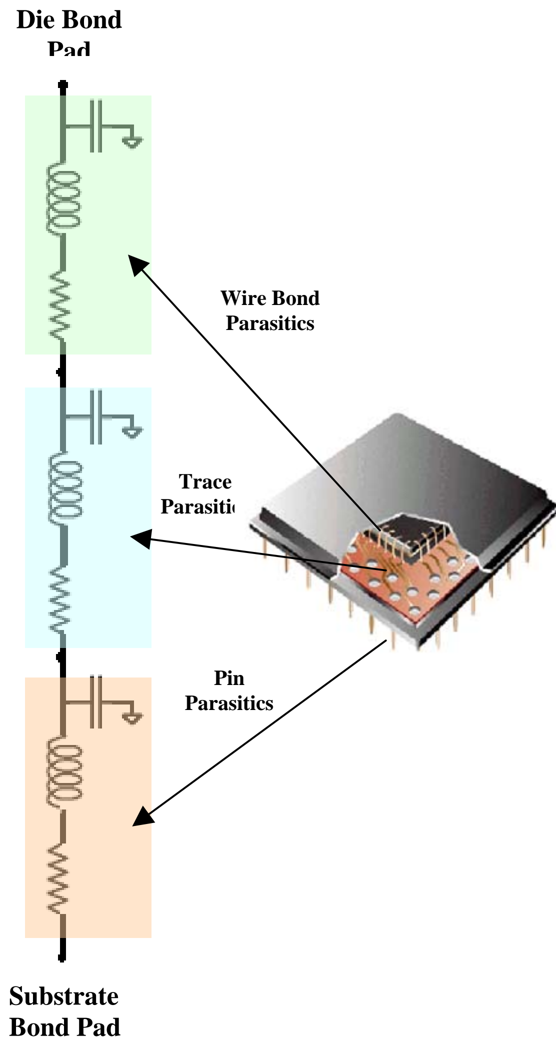

Figure 7. Component-level packaging electrical parasitics (Source: Terman [3]).

lengths by eliminating substrate routing and additional wire bond interconnects.

IC/DT™ is designed to reduce noise and crosstalk within the CCA and from the external environment. Large ground and power planes minimize crosstalk between conductors internal to the CCA. Large planes used for power and ground distribution in IC/DT™ increases the cross-sectional surface area of the conductor, reducing attenuation of the signal as a result of large line/plane resistances. Trace width and spacing is similar to that of SMT design reducing the opportunity for noise on adjacent signals. Internal core/layer and pre-preg materials are also similar to that of SMT with like dielectric constants and dissipation factor.

Typical dielectric materials used for THMA or SM design are in the form of solder mask that acts as an insulating blanket over surface conductors. A better dielectric coating, meaning lower dissipation factor and dielectric constant in addition to higher electrical resistivity, is used in IC/DT™ that provides complete and uniform coverage. This

dielectric conformal coat binds to all external surfaces uniformly, including edges, rendering all surfaces insulative. It provides complete environmental and electrical protection of all conductors and surfaces. Encapsulation of the cavities followed by a final seal with a Cu lid provides EMI shielding from the environment. These factors all contribute to coupled noise, or lack there of, within a CCA.

CHALLENGES

As with all new and emerging technologies, there are many challenges that exist. As was faced by the MCM designers in the early nineties and System in Package (SiP) designers today, obtaining known good die is a challenge. There are many different tiers of known good die (KGD), and distinguishing between the differences is essential. Also, similar function IC's fabrication masks differ amongst IC manufacturers. This can affect die bond location and overall size of the die. Burn-in of singulated die prior to assembly is very costly. IC/DT™ requires tight process control and decreases reworkability as a full-up assembly. However as technology moves toward more frequent use of bare die as shown by the increase in stacked-die packages and SiP, more efficient and inexpensive methods will develop for providing KGD. Die distributors are answering the call for more reliable die by offering testing services using Temporary Wire Bond (TWB), SoftTAB™, DiePak™, and wafer probing. Industry standards, JEDEC 49 and IEC 62258, are currently being developed for the procurement, shipping, and handling of bare die [5].

CONCLUSION

Imbedded Component / Die Technology will revolutionize the packaging of electronics for high reliability applications. By eliminating external packaging of components and optimizing placement, one can achieve a smaller form and fit factor as well as a reduction in mass. Imbedding components in a substrate in a 3D state maximizes the component-to-substrate ratio making available CCA size reduction or system functionality/redundancy addition. The use of a copper cooling core provides a rigid platform for mounting die and components in addition to thermal relief. Flexible interconnects improve electrical/mechanical reliability by distributing applied stresses across the connections coupled with a vibration-dampening medium. This design methodology equates to a lighter, smaller CCA while offering the highest degree of reliability.

Jim Raby, P.E., Mark McMeen, and Jason Gjesvold

REFERENCES

[1] Prasad, R.P., *Surface Mount Technology – Principles and Practice*. Norwell, MA: Chapman & Hall.

[2] Harman, G.G., *Wire Bonding in Microelectronics – Materials, Processes, Reliability, and Yeild*. New York, NY: McGraw-Hill.

[3] Terman, C.J., *Fall 2002 Course 6.371 Packaging Presentation.* Retrieved August 3, 2003 from http://6371.lcs.mit.edu/

[4] Doane, D.A., Franzon, P.D. (Eds.). (1993). *Multichip Module Technologies and Alternatives – The Basics.* New York, NY: Van Nostrand Reinhold.

[5] Die Products Consortium. (2003, October). *DPC Projects: Standards Project.* Retrieved December 2, 2003,from http://www.dieproduct.com/Projects/standards/standards.html